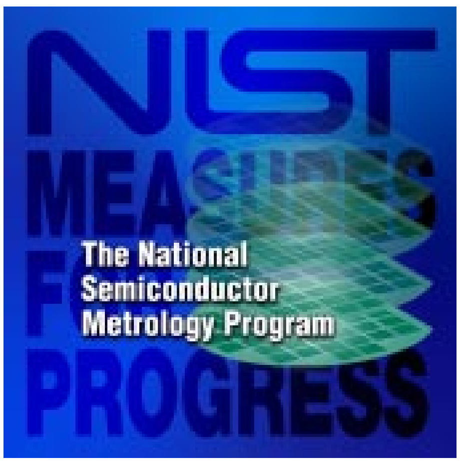
2.7 Microelectronics

The U.S. Industry & Trade Outlook '99 places the value of semiconductor shipments at nearly $200 billion, with metrology investments exceeding $3 billion. CSTL supports this industry by providing the necessary physical standards for process control, for parameters such as temperature and humidity. SRMs designed to standardize fabrication, as well as reliable kinetic and thermophysical property data to facilitate process modeling are critical to the semiconductor industry. Fast-paced development requires dramatically improved measurement tools to keep advanced microelectronic manufacturing competitive.

CSTL contributes to the NIST National Semiconductor Metrology Program (NSMP). The Semiconductor Industry Association requested that the Department of Commerce form the NSMP in support of its National Technology Roadmap for Semiconductors. The NSMP is managed by the Office of Microelectronic Programs (OMP) of the NIST Electronics and Electrical Engineering Laboratory.



The NSMP conducts, often with industrial collaborators, projects associated with chip lithography, interconnectivity, materials and bulk processes, and packaging. NSMP draws on a full range of NIST expertise in semiconductor metrology to meet the metrology needs of materials, equipment, instrument, and device manufacturers. Projects focus on mainstream silicon CMOS (complementary metal-oxide semiconductor) technology addressed by the National Technology Roadmap for Semiconductors. CSTL competencies in several areas contribute to metrology development needs in semiconductor manufacturing. Working with the OMP, CSTL develops, evaluates, and validates process measurement technologies important in semiconductor manufacturing. Several projects support advances in semiconductor metrology focused on specific manufacturing technologies where metrology issues must be resolved to realize goals set by the industry.

Standards for Process Control

Surface Temperature Measurements using RTP

K.G. Kreider, C.W. Meyer, V. P. Scheuerman, W.C. Ausherman (836), D.P. DeWitt, and B.K. Tsai (PL)

The goal of the CSTL work is to improve the accuracy of wafer surface temperature measurements, with emphasis in the area of rapid thermal processing (RTP) of semi-conductors. The semiconductor manufacturing industry requires improved process measurement accuracy of silicon wafer temperatures due to increasingly stringent dopant diffusion requirements critical to product quality and device performance. As a result, the industry has an uncertainty requirement of 2 °C at 1000 °C for RTP for the future generation of semiconductor devices

> ***Technology Transfer:***
>
> **NIST/CSTL cooperative project with SEMATECH, University of Texas, and Sensarray, Inc. has included both the design, fabrication, testing, calibration, and delivery of two thin-film calibration wafers.**
>
> **Thin-film wafers have been provided to Applied Materials and Vortek Industries for testing in commercial RTP tools.**
>
> **The NIST patent on the "Temperature calibration wafer for rapid thermal processing using thin-film thermocouple" was issued Mar. 14, 2000 and licensed to Watlow Gordon Inc. for commercial production.**

Light pipe radiation thermometers (LPRTs) are non-contacting and the sensor of choice in RTP. Thermocouple instrumented wafers are used to calibrate LPRTs in-situ. NIST efforts are based on combinations of stable thin-film and Pt/Pd wire thermocouples (TCs). The use of thin-film TCs (TFTCs) minimizes errors arising from much larger heat transfer effects present with other types of contact temperature sensors. This technique permits an expanded uncertainty of less that 1 °C when the wafer temperature is uniform to within 10 °C. Additionally, the effect of the environment of LPRT response was investigated to improve calibration procedures. Previously, TFTCs were shown to be useful up to 900 °C. Recently we found that by increasing the thickness of the underlying SiO_2 layer from 310 nm to 690 nm, operating temperatures up to 1000 °C could be achieved with a standard uncertainty target of 0.4 °C. Future work includes design improvement to reduce the uncertainty in temperature measurement between 700 °C and 1000 °C.

Standards for Low Concentration of Water Vapor in Gases

J.T. Hodges, G.E. Scace, P.H. Huang, W.W. Miller (836), and D.C. Hovde (Southwest Sciences)

Details provided in the **Process Metrology** section.

Improving Precision of Humidity Measurements with Absorption Spectroscopy

J.T. Hodges (836)

Details provided in the **Process Metrology** section.

Quantitative Measurements for Vacuum Process Control

J.P. Looney, R.F. Berg (836), and D.S. Green (University of Maryland)

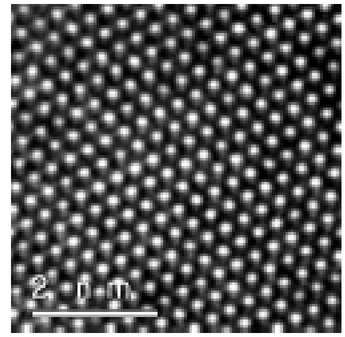
> **Quantitative, real-time, in-situ measurement capability for semiconductor process-control combines expertise in optical diagnostics and flow calibration techniques.**

The increasing volume and complexity of vacuum processing, most notably in the semiconductor industry, requires real-time monitoring and control of process gases, reaction products, and gaseous contaminants. Our previous work demonstrated that residual gas analyzers (RGAs) could be made quantitative for *in-situ* monitoring of reaction products, but the ± 5% to 10% imprecision (from analyte generation in the ionizer) was too large for process control, as is variability among mass flow controllers. Optical techniques are promising for real-time monitoring, but realizing their potential requires a better understanding of the factors limiting their performance. Researchers in CSTL's Process Measurements Division began developing an advanced chemical process monitor based on cavity ring-down spectroscopy (CRDS) to quantify the HF generated in the thermal chemical vapor deposition (CVD) of tungsten metal films (WF_6 in an H_2-rich environment). Our approach is to establish compact, low-cost, and robust optical diagnostic hardware at NIST, then transition it to Prof. Gary Rubloff's CVD facility at the University of Maryland for process control trials. With CRDS, we expect to achieve the desired measurement precision, and hope to use it to improve other detection methods such as RGAs.

Electron Microscopy to Measure Gate Dielectric Films on Silicon

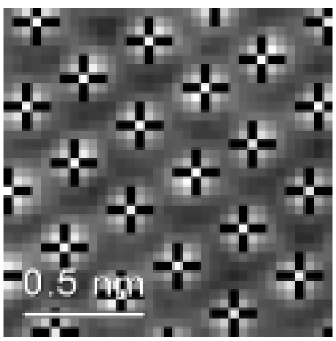
J.H.J. Scott (837)

Ultrathin films of silicon dioxide (SiO_2) and silicon oxynitride (SiO_xN_y) on silicon substrates are used widely in the semiconductor industry as gate dielectrics in CMOS transistors. As gate dielectric thickness requirements fall well below the 100 nm level, oxide fabrication tools must produce films with a thickness tolerance of less than 0.3 nm. Metrology tools with a precision of better than 0.1 nm are required. To evaluate high resolution TEM as a thickness measurement technique, blanket films of dielectric grown on silicon were obtained from SEMATECH. TEM samples were prepared in cross section by mechanical dimpling and ion milling, and high resolution micrographs were acquired at 300 keV using a CCD camera (see figure to right). Digital image processing was used to calibrate the magnification (using the silicon substrate as an internal standard), identify the dielectric film boundaries, and extract the film thickness.



High resolution transmission electron micrograph (TEM) of single crytsal silicon beneath an ultrathin dielectric film

New methods were developed for obtaining two-dimensional calibration information from a lattice image of the silicon substrate. The atomic plane spacings were measured with sub-pixel accuracy by locating peaks using a weighted center-of-mass algorithm (see figure to left), followed by a least-squares fit of lattice basis vectors. The film/substrate interface was located using integrated intensity profiles. Films nominally 2 nm thick were measured with an estimated uncertainty of 0.2 nm.

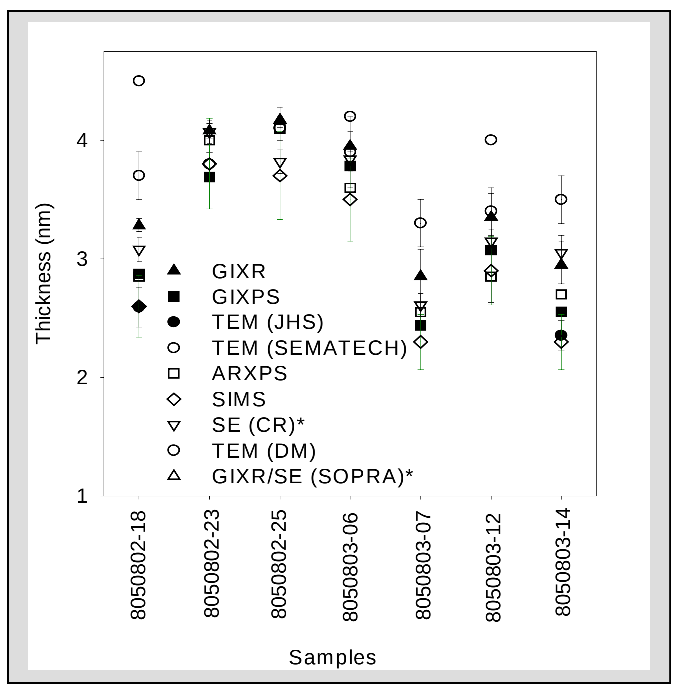


Crosses mark the recorded position of each intensity peak. Weighted-centroid fitting allows atomic spacings to be determined with sub-pixel precision

Thickness Measurements of SEMATECH Gate Dielectrics by GIXPS

T. Jach and E. Landree (837)

Standard methods of determining the thickness and composition of gate dielectric materials for CMOS devices on silicon encounter difficulties when the total layer thickness is less than 100 nm. A recent measurement by six techniques of silicon oxynitride samples circulated by SEMATECH pointed to variations between the total measured thickness on the order of 50%.



A new method of grazing incidence X-ray photoelectron spectroscopy (GIXPS), as developed at the NIST synchrotron radiation beamline X-24A at Brookhaven National Laboratory, is highly suitable for analyzing the complex heterogeneous layers in the gate dielectric materials. The X-ray photoemission provides chemical analysis of the elements present in the layers, and the behavior of the X-ray fields at the grazing incidence provide thickness information.

Seven samples from SEMATECH that had been measured by other techniques with significant variations in results were measured and analyzed using GIXPS. Analysis of the data shows thicknesses that lie near the middle of the spread determined by the other methods. We also performed analyses to estimate the variation in results expected due to inaccuracies of the published physical parameters that go into fitting the data. GIXPS fits of certain samples which had resisted interpretation by methods such as ellipsometry, angle-resolved X-ray photo-emission spectroscopy, and X-ray reflectivity indicate the formation of an unexpected surface nitride layer. The accuracy of the results will be tested by varying some of the parameters (X-ray energy, composition) in a controlled manner. Since, there is general correlation in the thickness measurements among different methods the reasons for discrepancies should be discernable.

Fabrication and Electron Microprobe Characterization of Barium-Strontium-Titanate Films
R.B. Marinenko, J. Armstrong (837), D.L. Kaiser, J.J. Ritter, P.K. Schenck, C. Bouldin, J.E. Blendell, and I. Levin (MSEL)
Details provided in the **Nanotechnology** section.

Ultra Shallow Depth Profiling of Dopants with ToF-SIMS
A.J. Fahey and S.V. Roberson (837)
Details provided in the **Nanotechnology** section.

Kinetic Instabilities Due to Step-Edge Barriers on Plasma-Etched GaAs.

S.W. Robey (837)

Surface morphology development during non-equilibrium processes, such as thin film growth or etching, is the result of a complex interplay between a number of dynamic processes, including surface diffusion, desorption, and gas phase diffusion. Several techniques (photoelectron spectroscopy, reflection high energy electron diffraction, etc.) are employed in tandem to study plasma etching, with the bulk of the effort focused on analysis of data from atomic force microscopy (AFM). Analysis of time and spatial correlation functions and higher order moments of the statistical distribution for the surface height provides clues to the dominant surface dynamics and the length scales over which they are important. The data are compared with the results of continuum models or Monte-Carlo simulations for the surface dynamic processes.

Understanding of the complex surface dynamics that determine surface morphology (on an ≈ 10 nm to 1000 nm length scale) during plasma etching of semiconductor surfaces is an important aspect of semiconductor processing. Achieving a desired morphology, over pertinent length scales, is often a key factor determining success or failure in the development of a surface process.

Above 600 K, the surface morphology displays a gradually decreasing anisotropy, with the surface anisotropy disappearing by about 700 K. The instability below 600 K is most likely associated with the existence of additional barriers to surface diffusion at step edges, Ehrlich-Schwoebel (ES) barriers. An interesting feature is that the transition temperature occurs in the range where it is expected that desorption of surface hydrogen would become important, suggesting a potential link between the appearance of a step edge barrier and surface hydrogen. Future work will examine the detailed temperature and time dependent behavior with the goal of identifying whether the instability is in fact due to step-edge barriers, refining the estimate for this barrier, and identifying the potential role of hydrogen.

Work to date has focused on the kinetic roughening of the GaAs (001) surface during H_2 and CH_4/H_2 plasma etching as a function of time, surface temperature, and gas composition, to identify dominant physical processes controlling the surface morphology and establish connections between surface morphology and specific microscopic surface processes. For length scales below 50 nm to 100 nm (depending on substrate temperature), the surface morphology is dominated by diffusion dynamics. For larger length scales, there is a crossover and desorption/etching effects dominate.

Standards for Ion-Implantation in the Production of Semiconductor Wafers

R.R. Greenberg, R.M. Lindstrom (839), and D.S. Simons (837)

Ion implantation is a key technology for the semiconductor industry, with spatial-concentration profiles characterized typically by secondary ion mass spectrometry (SIMS), a technique that requires standards for calibration. The variability among results for recent interlaboratory comparisons has demonstrated a real need within the industry for these standards. An accuracy-based standard would permit the transfer of technology from one manufacturing site to another, and would allow a more useful comparison of experimental data with theoretical process models.

The SEMATECH Analytical Managers' Working Group identified the development of the Arsenic in Silicon SRM as one of their top priorities for implants in silicon.

A CSTL team with scientists from two divisions produced a new silicon wafer SRM that has been certified for total dose of implanted ^{75}As per unit area, to meet the needs of the semiconductor industry. Additional information about the concentration of As atoms as a function of depth below the surface was provided by SIMS. The arsenic content was certified using instrumental neutron activation analysis (INAA) as a primary method. Since variability of SIMS measurements can be kept to within a few percent when the measurement process is carefully controlled, the relative (expanded) uncertainty for the arsenic certification in the SRM was targeted at ≤1 % on a relative basis. To achieve this level of accuracy, and to document the actual expanded measurement uncertainty, each individual uncertainty source was explicitly evaluated. A total of 29 individual uncertainty components were evaluated, and the final relative expanded uncertainty achieved was 0.38% for a total arsenic content of 90 ng/cm^2. The largest individual source of measurement uncertainty was observed to be that of the amount of arsenic in the calibration solutions.

Completion of SRM 2134 complements SRM 2137, Boron in Silicon, which was released in 1998. These SRMs are used by the semiconductor industry to underpin critical dopant concentration and depth measurements that are essential to successful device manufacturing.

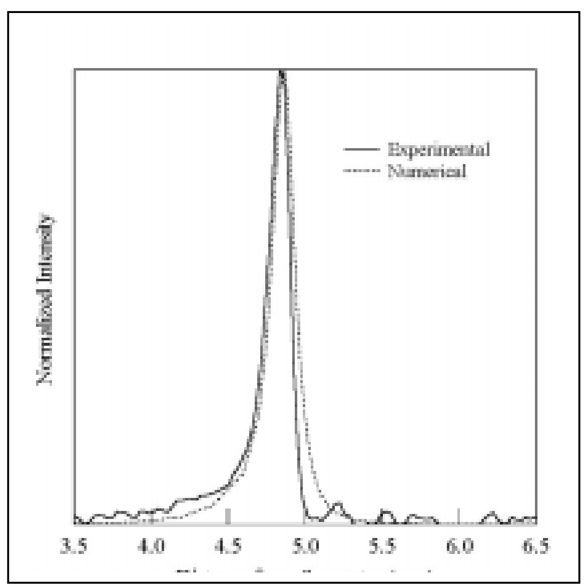
Models and Data for Semiconductor Processing

Application of Process Models and Controllers to Semiconductor Processing

R. W. Davis, J.E. Maslar, E.F. Moore (836), D.R. Burgess, Jr. (838), R.L. Axelbaum (Washington University), and S.H. Ehrman (University of Maryland)

CSTL provides the necessary information and scientific infrastructure to enable the application of semiconductor process models and controllers that are well-grounded in fundamental physical laws.

Process simulation has the potential to significantly enhance the design phase of process development so as to improve both efficiency and quality. This is because computational power has evolved to the point where highly sophisticated models can be constructed for a variety of complex semiconductor processes. However, the increasing complexity of these models implies a greater need for accurate fundamental thermochemical and kinetic data, which are not presently available. CSTL's approach is both to develop and use methods for reliably generating the data necessary for validation of process modeling. The reliability, quality, and utility of the generated data must also be demonstrated to the user community. Consequently, the development of process models of wide applicability is essential, as is model validation carried out in reference reactors prototypical of industrial processing equipment.



Gas phase formation of particles is a significant source of microcontamination in CVD reactors. Models predicting particle nucleation, growth, and evolution have been developed and incorporated in a CVD reactor model for polysilicon deposition from silane. Particle scattering intensities were measured experimentally, and these intensity profiles were compared with those generated numerically by the semi-empirical NIST microcontamination model.

The NIST model contains two empirical parameters related to thermophoretic force and condensational sticking coefficient. With these parameters properly chosen, the numerical versus experimental comparisons are excellent, as shown in the figure. A new web site has been established to disseminate this information in a public forum. Data related to the bond dissociation energies obtained during the decomposition of fluorinated ethanes, as well as decomposition rates for organometallic CVD precursors, will be part of the database compilation.

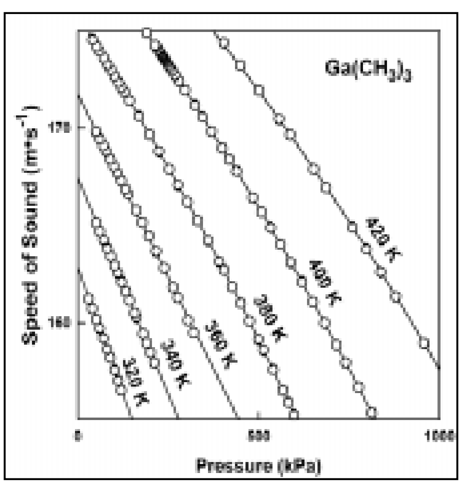
Thermophysical Properties of Gases used in Semiconductor Processing

J.J. Hurly, K.A. Gillis, and M.R. Moldover (836)

CSTL provides improved standards and data for mass flow controllers including improvement in low-range gas flow standards and provision of transport property data for chemically reactive process gases.

Mass flow controllers (MFCs) are numerous and ubiquitous in semiconductor manufacturing. A major use of MFCs is to control reactant feeds to most gas phase processes where accuracies in their concentration is critical to success. The semiconductor industry requires high-accuracy data for modeling CVD (chemical vapor deposition) processes and for calibration of MFCs (mass flow controllers). Many process gases used in wafer processing are toxic, corrosive, and/or pyrophoric. MFCs are often calibrated with benign “surrogate” gases (*e.g.* N_2, CF_4, SF_6, or C_2F_6) but are used to deliver process gases (*e.g.* Cl_2, HBr, BCl_3, WF_6). Adjustments of MFC response to account for the differences between the non-reactive and reactive gases can be accomplished when the thermophysical properties of both are known with sufficient accuracy. The thermophysical property data for reactive process gases are sparse and rarely accurate. Accurate thermophysical property data are also required to model the gas streams that are used in CVD processes. (For example, models are needed for the velocity, temperature, and concentration profiles in the vicinity of a hot susceptor.)

NIST is using acoustic techniques to measure the thermophysical properties of the process gases, the "surrogate" gases, and binary mixtures of process and carrier gases.



For example, the speed of sound in $(CH_3)_3Ga$ (a pyrophoric organo-metallic) and NF_3 (an aggressive oxidizer) was measured in a specially designed facility at NIST. These two gases were given high priority by the SEMATECH MFC Working Group. The figure to the left displays speed-of-sound data for $(CH_3)_3Ga$ (trimethlygalllium). Typically, the data range from below the boiling temperature to 200 °C and from 25 kPa to 1500 kPa or 80% of the vapor pressure. The acoustic data are analyzed to determine the ideal-gas heat capacity and the equation of state with uncertainties of approximately ± 0.1%. Model pair potentials are also derived from the data. These models are used to reliably extrapolate the equations of state to temperatures above 1000 K and to estimate the transport properties.

A new NIST database is available that provides the heat capacity, thermal conductivity, viscosity, and the virial coefficients for the virial equation of state providing the pressure-density-temperature relation for the process gases.

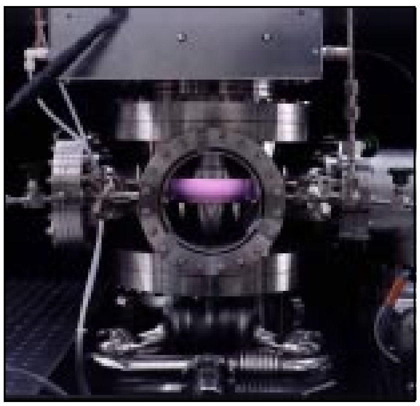
Measurements and Models for Plasma Processing

M. Sobolewski and K. Steffens (836), J. Olthoff, Y. Wang, L. Christophorou, A. Goyette (EEEL), and E. Benck (PL)

Advanced chemical and electrical measurement methods and models are needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in process optimization, process control, and model-based reactor design.

Model-based process design and control are important needs identified in the *National Technology Roadmap for Semiconductors*.

CSTL's Process Measurements Division, in collaboration with researchers from EEEL and PL, have made use of reference reactors as a testbed for validating models and testing new measurement techniques. The reactors, known as Gaseous Electronics Conference Radio-Frequency Reference Cells (GEC Reference Cells), provide a well-defined basis for comparison of measurements between laboratories. The cells are equipped with a wide variety of plasma diagnostic tools, which measure the chemical, physical, and electrical properties of plasmas. Information provided by the set of diagnostics allows testing of models. Also, sensors designed for manufacturing environments can be installed on the cells and compared with diagnostic results.



Work continues on the development of sensors for real-time monitoring of ion current and ion energy in plasma reactors. These sensors are based on rf electrical measurements, which are interpreted using models for the electrical properties of plasma sheaths. This year, a two-sheath model was developed which allows the ion energies at both the powered and grounded electrodes to be monitored simultaneously. The model was validated by comparison to measurements of sheath voltages at both electrodes and ion energy distributions at the grounded electrode. We continue to investigate 2-D species densities in the GEC Reference Cell using 2-D planar laser-induced fluorescence (PLIF) imaging. In these studies, the concentration of CF_2 in fluorocarbon etching and chamber-cleaning plasmas is monitored as a marker of uniformity and chemistry for validation of 2-D plasma models.

Recent measurements have characterized the effect of varying electrode gap on CF_2 uniformity and density. Present investigations focus on the effect of increased plasma power and the presence of a silicon wafer on the spatially-resolved CF_2 density.